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| Jeffrey Huter c/o Blakely, Sokoloff, Taylor, & Zafman LLP 12400 Wilshire Boulevard, Seventh Floor Los Angeles, CA 90025 | | EXAMINER TRUJILLO, JAMES K | | |
| | | ART UNIT 2116 | | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

09/893,718

Applicant(s)

NALAWADI ET AL.

Examiner

James K. Trujillo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file:
Preliminary Amendment dated 8/2/2001, Change of Address dated 06/26/2003, Change in Power of Attorney dated 09/02/2003, Drawings dated 11/17/2003.
2. Claims 1-40 are presented for examination.

Claim Objections

3. Claim 28, 34 and 39 are objected to because of the following informalities: Claims 28, 34 and 39 recite an error correction code memory and initializing thereof. It appears that specification does not support an error correction code memory or initializing such a memory. Other claims recite detecting physical memory error checking and correction capability. It appears that the applicant should rephrase the above claims to recite something to the effect executing error checking and correction code to initialize memory. For the purposes of examination it will be assumed that error checking and correction code is executed to initialize memory. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 3, 5-7, 25, 31 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins, U.S. Patent 6,158,000 in view of Levy et al., U.S. Patent 6,314,511.
6. As to claim 1, Collins substantially teaches a computer system comprising:
- a. a host chipset (memory controller, north bridges 116 and 117) connected to the processor [figure 2];
 - b. PCI devices (at least a video card) connected to the host chip set, via a PCI bus (buses 118 and 119) [figure 2 and col. 5 lines 7-15 and col. 5 lines 61-67]; and
 - c. a main storage (main memory 115 and BIOS ROM) connected to the host chipset and arranged to store an operating system (OS) (locates and executes OS – the OS is usually stored in main memory when it is loaded and executed) [col. 7 lines 52-55] and contain a basic input/output system (system BIOS) [col. 1 lines 56-60] configured to execute multiple pre-boot tasks [col. 7 lines 56-65], including memory initialization (verify and clearing memory) [col. 7 line 66 through col. 8 line 19] and PCI bus initialization (when initializing a PCI device) [col. 9 lines 37-41] concurrently (BSP performs POST tasks while AP performs memory tests) [col. 8 lines 20-34 and col. 9 lines 23-36], before passing control to the operating system (OS) (load/run OS 324 after initializations) [figure 3].

Specifically, the system of Collins uses at least two processors (a BSP and an AP) to concurrently perform two different initialization tasks before the OS receives control of the system. In Collins the booting time of the system is reduced. Collins uses multiple physical processors.

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Levy substantially teaches a computer system having a processor equipped to serve as multiple logical processors (by using simultaneous multithreading architecture (SMT)) [col. 8 lines 30-39]. As is well known in the art, simultaneous multithreading allows a single processor to serve as multiple logical processors in that simultaneous multithreading allows a processor to concurrently execute multiple threads as if it had multiple processors without actually having multiple processors. In concurrently executing multiple threads, the processor appears to act as multiple processors to the rest of the system and is thus interpreted as multiple logical processors. The system of Levy is a generic computer system. Levy teaches that his implementation of the SMT obtains a desired advantage in speedups over two and four processor multiprocessors systems [col. 10 lines 15-32].

It would have been obvious to one of ordinary skill in the art, having the teachings of Collins and Levy before them at the time of the invention to modify the system of Collins by replacing the multiple processors of Collins with the processor having SMT of Levy resulting in the basic input/output system configured to execute multiple boot tasks, including memory initialization and PCI bus initialization concurrently on the processor which serve as multiple logical processors. One of ordinary skill in the art would have been motivated to make this modification to further reduce the time to boot-up the computer system such as that of Collins in view of the teachings of Levy.

7. As to claim 3, Collins together with Levy substantially taught the computer system according to claim 1 as described above. Collins together with Levy further teaches wherein said processor equipped to serve as multiple logical processors (as taught by Levy) allows the system BIOS to execute the memory initialization on one of the logical processors (AP) while enabling

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the other logical processor (BSP) to proceed with PCI bus initialization tasks (other POST tasks) [col. 8 lines 20-34]. Specifically, as modified by Levy, the system of Collins would now use logical processors instead of physical processors.

8. As to claim 5, Collins together with Levy substantially taught the computer system according to claim 1 as described above. Collins together with Levy does not expressly disclose wherein said processor equipped with logical processor allows the system BIOS to execute the PCI bus initialization on one of the logical processors while enabling the other logical processor to proceed with other normal PCI device initialization tasks. In summary, Collins discloses only two processors being initiated to concurrently perform two tasks.

Those of ordinary skill in the art will appreciate that initiating more processors for concurrently tasks appropriately would further reduce the time for booting. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Collins by enabling one processor to execute PCI bus initialization while enabling the other processors to proceed with other normal PCI device initialization tasks.

9. As to claim 6, Collins together with Levy substantially taught the computer system according to claim 3 as described above. Collins further teaches initializing PCI devices [col. 9 lines 39-41]. Collins describes initializing PCI devices. It is interpreted that one of ordinary skill would have understood that this is to mean all PCI devices. In order to initialize the PCI devices it is necessary to scan the buses for each device (determining PCI device addresses). In initializing the devices it is also necessary to initialize all possible PCI functions otherwise the device would not be truly initialized. Collins teaches that the BSP continues with POST tasks, which include PCI device initialization, and then waits for memory tests [col. 8 lines 28-30]. It

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appears that at that point Collins has terminated initializing all the PCI buses and devices because all buses and devices have been initialized. Even if Collins does not initialize all the PCI buses and devices it would have been obvious to one of ordinary skill in the art to do so because doing so would allow the system to be ready for the operating system.

10. As to claim 7, Collins together with Levy teaches the computer system according to claim 1 as described above. Collins modified by Levy teaches a Boot-Strap Logical Processor (BSLP) (BSP) assigned to execute a set of pre-boot tasks and one or more Alternative Logical Processors (ALP) (AP) assigned to execute another set of pre-boot tasks concurrently until all assigned pre-boot tasks are completed before passing the control to the operating system (OS) [col. 8 lines 20-34]. Specifically, Collins teaches using at least two physical processors (BSP and AP) to concurrently execute at least two pre-boot tasks. In Collins as modified by Levy, the processors (BSP and AP) would be logical processors.

11. As to claim 25, Collins substantially teaches a system comprising:

- a. a memory (BIOS ROM) comprising first instructions associated with a first startup initialization task and second instructions associated with a second startup initialization task (BIOS with multiple modules) [figure 2 and col. 6 lines 8-18]; and
- b. a processor (AP) to execute the first instructions associated with the first startup initialization task (POST tasks) and a second processor (BSP) to initiate execution of the second instructions (memory test) associated with the second startup initialization task prior to completing execution of the first instructions [col. 8 lines 20-34].

Specifically, Collins teaches executing first and second instructions associated with first and second initialization tasks respectively. Collins is different from the claimed invention in that the claimed invention uses a single processor while Collins uses at least two different processors.

Levy teaches a system wherein one processor may execute first and second instruction for first and second tasks respectively [col. 8 lines 30-39]. In summary, Levy teaches a system that may execute multiple tasks (threads) simultaneously using simultaneously multithreading technology (SMT). As is known to those of ordinary skill in the art, simultaneous multithreading executes tasks (threads) as if each task were executing on its own processor. The system of Levy is directed toward a general computer system. Levy further teaches that his implementation of the SMT obtains a desired advantage in speedups over two and four processor multiprocessors systems [col. 10 lines 15-32].

It would have been obvious to one of ordinary skill in the art, having the teachings of Collins and Levy before them at the time of the invention to modify the system of Collins by replacing the multiple processors of Collins with the SMT processor of Levy resulting in a single processor to execute the second of instructions prior to completing execution of the first instructions. One of ordinary skill in the art would have been motivated to make this modification to further reduce the time to boot-up the computer system such as that of Collins in view of the teachings of Levy.

12. As to claim 26, Collins together with Levy taught system according to claim 25 as described above. Collins teaches that a first processor (AP) executes the first instructions and a second processor (BSP) executes the second instructions. As modified by Levy the first and

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second processors would be logical processors because in using the SMT the single processor executes tasks as if each task were executing on its own processor (logical) but not an actual physical processor.

13. As to claim 27, Collins together with Levy taught system according to claim 25 as described above. Collins further teaches a second memory (main memory 115) wherein the first instructions in response to being executed result in the processor initializing the second memory [figure 2 and col. 8 lines 24-31].

14. As to claim 28, Collins together with Levy taught system according to claim 25 as described above. Collins further teaches error checking and correction code (writing test patterns), wherein the second instructions in response to being executed result in initializing the memory [col. 7 lines 66 through col. 8 lines 19].

15. As to claim 29, Collins together with Levy taught system according to claim 25 as described above. Collins further teaches wherein the system comprises a peripheral bus and associated devices, wherein the first instructions in response to being executed result in the processor initializing the peripheral bus and associated device (BSP continues with other POST tasks) [col. 8 lines 28-34 and col. 9 lines 37-41].

16. As to claim 30, Collins together with Levy taught system according to claim 25 as described above. Collins further teaches the system further comprising a peripheral bus and associated devices (PCI buses and devices) [figure 2, col. 5 lines 13-15 and col. 9 lines 37-41]. Collins further teaches wherein the first instructions in response to being executed result in the processor initializing the peripheral component interconnect bus and associated devices [figure 2, col. 5 lines 13-15 and col. 9 lines 37-41]. In initializing the PCI devices it is inherent that their

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buses would also be initialized because Collins is directed toward system initialization. Even it is not inherent that the PCI buses are initialized when the devices are initialized it would have been obvious to do so in order to ensure that incorrect or corrupted data is not sent to the device.

17. As to claim 31-40, Collins together with Levy taught the claimed system therefore together they also taught the claimed method and the claimed computer readable medium.

18. Claims 2, 12-13, and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins and Levy and further in view of Hobson et al., U.S. Patent 6,115,813.

19. As to claim 2, Collins together with Levy substantially teach wherein the computer system according to claim 1 as described above. Collins further teaches wherein said main storage comprises:

- a. a main memory arranged to store the operating system for use by the processor (the main memory 115 of Collins, as is known to those of skill in the art, would store the operating system when it is loaded so the processor can quickly access it) [figure 2];
- b. a flash memory arranged to store the system BIOS (BIOS ROM 124) [col. 6 lines 8-24].

Collins and Levy does not discuss wherein flash memory arranged to store the BIOS also stores other applications that may execute during boot up before the operating system is loaded. As is well known to those of ordinary skill in the art, a BIOS ROM generally refers to a flash memory that holds BIOS. Even if the BIOS ROM of Collins was not a flash memory it would have been obvious to those of ordinary skill in the art at the time of the invention to modify the

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BIOS ROM of Collins by replacing it with a flash memory to hold the BIOS. Doing so would allow the BIOS to be easily updated without having to obtain new hardware thereby reducing cost.

Hobson teaches wherein other applications flash memory arranged to store the BIOS also stores other applications (ACPI instructions) that may execute during boot up before the operating system is loaded [figure 2 and col. 2 lines 47-54]. Hobson is directed to booting a system similar to that of Collins. The system of Hobson desirably allows power management to be implemented upon booting of the system in either an ACPI mode or non-ACPI mode [col. 1 lines 44-51].

It would have been obvious to one of ordinary skill in the art, having the teaching of Collins, Levy and Hobson before them at the time the invention was made, to modify the BIOS ROM as taught by Collins to further include ACPI instructions to allow the system to be booted in either ACPI or non-ACPI mode. This would allow power management to be enabled in legacy systems.

20. As to claim 12, Collins together with Levy and Hobson substantially teach computer system according to claim 2 as described above. The limitations of claim 12 are substantially the same as those of claim 2 and are therefore rejected for the same reasons.

21. As to claims 13 and 15-17, they appear to recite limitations previously addressed in the rejections of claims 3 and 5-7 and are therefore rejected by the same reasoning with respect to the cited references.

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22. Claims 4, 8-11 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins and Levy in further view of Intel Press Release and corresponding Datasheet.

23. As to claim 4, Collins together with Levy substantially taught the computer system according to claim 1 as described above. Collins further teaches wherein said memory initialization is executed by:

- a. a detecting a physical memory array (memory 115) plugged into the computer system (in order to write to the memory it must be detected) [col. 7 line 66 through col. 8 line 19];
- b. programming the controller with physical memory specifics, and initializing the physical memory using the controller [col. 7 lines 6-9];
- c. detecting a physical memory ECC capability (test patterns) [col. 7 line 66 through col. 8 line 19]; and
- d. programming the controller with the ECC capability, and writing zeros to the entire physical memory array [col. 8 lines 1-3] in order to ensure that memory is usable for the operating system (OS).

Specifically, Collins teaches initializing the memory through a memory controller.

Collins teaches testing the memory using ECC capability and then clears the memory prior to the OS accessing it.

The system of Collins is different than that of the claim invention in that the claimed invention recites a single host chipset to initialize the memory. As described by the applicants,

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the host chipset contains a memory controller and an I/O controller, which is similar to the north and south bridges of Collins.

The Intel Press Release, dated April 26, 1999, and corresponding datasheet (Intel 810 Chipset), discloses a chipset (Intel 810 Chipset) that integrates a memory controller and an I/O controller. According to the press release, the chipset offers improved reliability, ease-of-use and better multimedia performance.

It would have been obvious to one of ordinary skill in the art, having the teachings of Collins, Levy, the Intel Press Release and the corresponding datasheet before them at the time the invention was made, to modify the system of Collins by replacing the memory controller and the I/O controller of Collins with the single chipset as taught by the Intel Press Release and the corresponding data sheet. Modifying the system would result in improved reliability, ease-of-use and better multimedia performance.

24. As to claim 8, Collins together with Levy substantially teaches the computer system according to claim 7 as described above. Collins as modified by Levy further teaches wherein upon a system reset (power-on) said Boot-Strap Logical processor executes the following pre-boot tasks:

- a. detecting a physical memory (necessary for initializing memory), and programming a host chipset (configuring the memory controller) [col. 7 lines 5-9];
- b. detecting the presence of all logical processors and sending a SIPI (IPI) to wake up the Alternate Logical Processor (ALP) [col. 6 lines 43-46 and col. 8 lines 20-34];
- c. initializing all internal hardware of a host chipset, and all storage devices connected to a host chipset (necessary to initialize the system and devices) [col. 9 lines 37-38];

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- d. wait for ALP code execution to place the ALP in a wait state (AP is halted) before passing the control to the operating system [col. 8 lines 42-43 and figure 3].

The only difference between the system in Collins as modified by Levy and the claimed invention is that Collins teaches using multiple chipsets while the claimed invention recites only one chipset.

The Intel Press Release dated April 26, 1999 and corresponding datasheet (Intel 810 Chipset), discloses a chipset (Intel 810 Chipset) that integrates a memory controller and an I/O controller. According to the press release, the chipset offers improved reliability, ease-of-use and better multimedia performance.

It would have been obvious to one of ordinary skill in the art, having the teachings of Collins, Levy, the Intel Press Release and the corresponding datasheet before them at the time the invention was made, to modify the system of Collins by replacing the memory controller and the I/O controller of Collins with the single chipset as taught by the Intel Press Release and the corresponding data sheet. Modifying the system would result in improved reliability, ease-of-use and better multimedia performance.

25. As to claim 9, Collins together with Levy, the Intel Press Release and the corresponding datasheet substantially teach the system according to claim 8. Collins together with Levy further teach wherein upon receipt of the SIPI, said Alternate Logical Processor (ALP) (AP of Collins which would be a logical processor when modified as taught by Levy) executes the memory initialization [col. 8 lines 25-28] while the Boot-Strap Logical Processor (BSLP) (BSP of Collins which would be a logical processor when modified as taught by Levy) initializes all storage

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devices connected to the host chipset [col. 8 lines 28-34], and after memory initialization is completed, indicates to the Boot-Strap Logical Processor (BSLP) that the memory initialization are completed after all internal hardware of the host chipset and all storage devices connected to the host chipset are initialized by the Boot-Strap Logical Processor (BSLP) [col. 8 lines 25-34 and figure 3 (especially 328 and 330)].

The only differences between the claimed invention and Collins together with Levy, the Intel Press Release and corresponding datasheet is that the ALP of the claimed invention also performs PCI bus initialization and the BSLP of the claimed invention also performs initialization of internal hardware of the host chipset.

However, those of ordinary skill in the art will appreciate that the PCI bus and the internal hardware of the host chipset must be initialized when the system as (in order to prevent initial operation into an unknown state). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Collins together with Levy to assign the PCI bus initialization to the ALP (AP of Collins) and assign the initialization of the internal hardware to the BSLP (BSP of Collins). The bus and internal hardware initialization are tasks that are similar to those already done by Collins and it would result in the system being initialized into an known state.

26. As to claim 10, Collins together with Levy, the Intel Press Release and the corresponding datasheet substantially teach the system according to claim 9. Collins together with Levy does not expressly disclose wherein said processor equipped with logical processor allows the system BIOS to execute the PCI bus initialization on one of the logical processors while enabling the

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other logical processor to proceed with other normal PCI device initialization tasks. In summary, Collins discloses only two processors being initiated to concurrently perform two tasks.

Those of ordinary skill in the art will appreciate that initiating more processors for concurrently tasks appropriately would further reduce the time for booting. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Collins by enabling one processor to execute PCI bus initialization while enabling the other processors to proceed with other normal PCI device initialization tasks.

27. As to claim 11, Collins together with Levy, the Intel Press Release and the corresponding datasheet substantially teach the system according to claim 9. Collins further teaches initializing PCI devices [col. 9 lines 39-41]. Collins describes initializing PCI devices. It is interpreted that one of ordinary skill would have understood that this is to mean all PCI devices. In order to initialize the PCI devices it is necessary to scan the buses for each device (determining PCI device addresses). In initializing the devices it is also necessary to initialize all possible PCI functions otherwise the device would not be truly initialized. Collins teaches that the BSP continues with POST tasks, which include PCI device initialization, and then waits for memory tests [col. 8 lines 28-30]. It appears that at that point Collins has terminated initializing all the PCI buses and devices because all buses and devices have been initialized. Even if Collins does not initialize all the PCI buses and devices it would have been obvious to one of ordinary skill in the art to do so because doing so would allow the system to be ready for the operating system.

28. As to claims 22-24, Collins together with Levy, the Intel Press Release and corresponding Datasheet teach the claimed computer system. Therefore together they also teach the claimed computer readable medium.

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29. Claims 14 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Collins and Levy in further view of Hobson, Intel Press Release and corresponding Datasheet.

30. As to claims 14 and 18-20, claims 14 and 18-20 appear to recite limitations previously addressed and are therefore rejected for the same reasons as set forth hereinabove with respect to the cited references.

Conclusion

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,493,741 to Emer et al. This patent teaches a system that uses a simultaneous multithreaded processor

U.S. Pat. No. 6,038,632 to Yamazaki et al. This patent a system that uses interrupts to execute more than one tasks at a time.

S. J. Eggers et al, "Simultaneous Multithreading: A Platform for the Next-Generation Processors", IEEE Micro, September/October 1997, pages 12-18.

J. Lo et al. "Converting Thread-Level Parallelism Into Instruction-Level Parallelism via Simultaneous Multithreading", ACM Transactions on Computer Systems, August 1997, pages 322-354.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291 [new phone number may be in effect in mid October - (571) 272-3677]. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703)308-1159 [new phone number may be in effect in mid October - (571) 272-3670]. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
September 2, 2004


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